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10/682,277	10/08/2003	Darrell Rinerson	UNTYP024	9336

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/682,277	RINERSON ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 29-43* is/are rejected.

7)☒ Claim(s) *27,28 and 41* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 10/08/2003 is acceptable.

Claim Objections

2. Claim(s) 41 is/are objected to because it/they contain(s) typographical errors:

- **Claim 41**, line 4 recites:

"conductive lines **in** oriented in one direction"

which should be:

"conductive lines oriented in one direction"

- **Claim 41**, line 8 recites:

"the x-direction conductive lines and y-direction conductive lines;"

which should be:

"the x-direction conductive lines and y-direction conductive lines; **and**"

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1, 33, 38, and 41-42** are rejected under 35 U.S.C. 102(b) as being anticipated by Ovshinsky et al. U.S. Patent 5,296,716 (the '716 patent).

The '716 patent discloses in the figures and respective portions of the specification a conductive memory as claimed.

Referring to **claim 1**, the '716 patent discloses a conductive memory device comprising:

a conductive bottom electrode (32/34, Fig. 2);

a multi-resistive state element (36) arranged on top of and in contact with the bottom electrode, the multi-resistive state element having a resistivity; and

a conductive top electrode (38/40) arranged on top of and in contact with the multi-resistive state element;

wherein the resistivity of the multi-resistive state element may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes (column 5, lines 45-50 and Fig. 8); and

wherein at least one of the conductive electrodes functions as a barrier layer (column 12, lines 13-17).

Referring to **claim 33**, the '716 patent further discloses that at least one of the bottom electrode, the multi-resistive state element, or the top electrode is protected by an insulating barrier (encapsulating layer 44, Fig. 2).

Using the same reference characters and citations as detailed above and with reference to **claim 38**, the '716 patent discloses a conductive memory device, comprising:

a memory element that stores an adjustable resistive value;

two electrodes (32/34 and 38/40) that deliver current to the memory element;

wherein at least one electrode includes a terminal layer (40) that is suitable for connecting the electrode to either a conductive line (42) or a transistor terminal;

wherein the at least one electrode has an outside face that is defined by the terminal layer (40) and an inside face opposite the outside face; and

wherein the at least one electrode acts as a barrier layer.

Using the same reference characters and citations as detailed above and with reference to **claim 41**, the '716 patent discloses a re-writable memory comprising:

a substrate (50, Fig. 5);

a plurality of circuits (52) on the substrate;

a plurality of x-direction conductive lines (42, Figs. 2 and 4) oriented in one direction;

a plurality of y-direction conductive lines (12) in a different direction as the x-direction conductive lines, and crossing the x-direction conductive lines;

at least one memory array formed by memory cells placed substantially at the intersections of the x-direction conductive lines and y-direction conductive lines; and

wherein each memory cells in the memory array includes at least one electrode that acts as a barrier layer.

Using the same reference characters and citations as detailed above and with reference to **claim 42**, the '716 patent discloses that each memory cell includes a memory element (36) that stores an adjustable resistive value.

4. **Claims 1, 33-34, and 38-42** are rejected under 35 U.S.C. 102(e) as being anticipated by Gilton U.S. Patent Application Publication 20030193053 (the '053 publication).

The '716 patent discloses in Fig. 6B and respective portions of the specification a conductive memory as claimed.

Referring to **claim 1**, the '053 publication discloses a conductive memory device comprising:

a conductive bottom electrode (10, paragraph [0034]: "the bottom conducting line 10 comprises tungsten and acts as a bottom electrode");

a multi-resistive state element (18/20/24, chalcogenide material) arranged on top of and in contact with the bottom electrode, the multi-resistive state element having a resistivity; and

a conductive top electrode (26) arranged on top of and in contact with the multi-resistive state element;

wherein the resistivity of the multi-resistive state element may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes (paragraphs [0005], [0008], and [0009]); and

wherein at least one of the conductive electrodes functions as a barrier layer (paragraphs [0034] and [0042]).

Referring to **claim 33**, the '053 publication further discloses that at least one of the bottom electrode, the multi-resistive state element, or the top electrode is protected by an insulating barrier (12).

Referring to **claim 34**, the '053 publication further discloses that the insulating barrier (12) includes silicon nitride (paragraph [0035]).

Referring to **claim 38** and using the same reference characters and citations as detailed above, the '053 publication discloses a conductive memory device, comprising:

a memory element that stores an adjustable resistive value;

two electrodes (10 and 26) that deliver current to the memory element;

wherein at least one electrode includes a terminal layer (not shown in the figure but disclosed in paragraph [0042]) that is suitable for connecting the electrode to either a conductive line (28) or a transistor terminal;

wherein the at least one electrode has an outside face that is defined by the terminal layer and an inside face opposite the outside face; and

wherein the at least one electrode (26) acts as a barrier layer (paragraph [0042]).

Referring to **claim 39**, the '053 publication further discloses that only a portion of the at least one electrode (26) acts as barrier layer, the portion being located away from the outside face (paragraph [0042]: "In one aspect of the invention, a diffusion barrier (not shown), such as tungsten nitride, is deposited over the chalcogenide glass element 24 before forming the top electrode 26" and "[A]nother possibility is that the top electrode 26 is a multi-layered structure").

Referring to **claim 40**, the '053 publication further discloses that only a portion of the at least one electrode (26) acts as barrier layer, the portion being located away from the inside face

(paragraph [0042]: "A diffusion barrier may also be deposited over the top electrode 26" and "[A]nother possibility is that the top electrode 26 is a multi-layered structure").

Using the same reference characters and citations as detailed above and with reference to **claim 41**, the '053 publication discloses a re-writable memory comprising:

a substrate (8);

a plurality of circuits (not shown in the figure but disclosed in paragraph [0034]) on the substrate;

a plurality of x-direction conductive lines (10) oriented in one direction;

a plurality of y-direction conductive lines (28) in a different direction as the x-direction conductive lines, and crossing the x-direction conductive lines;

at least one memory array formed by memory cells placed substantially at the intersections of the x-direction conductive lines and y-direction conductive lines; and

wherein each memory cells in the memory array includes at least one electrode (26) that acts as a barrier layer.

Using the same reference characters and citations as detailed above and with reference to **claim 42**, the '053 publication discloses that each memory cell includes a memory element (chalcogenide material layer 18/20/24) that stores an adjustable resistive value.

5. **Claims 1, 8-10, 14, 18-19, 21-22, and 32** are rejected under 35 U.S.C. 102(e) as anticipated by Ignatiev et al. U.S. Patent 6,473,332 (the '332 patent).

The '332 patent discloses in Figure 1 and respective portions of the specification a conductive memory device as claimed. The '332 patent discloses an electrically operated, over-

writable, multi-valued, non-volatile resistive memory element (Abstract), and a memory element array including a plurality of the memory elements formed on a substrate in a column-row or array format (column 2, lines 53-56), the memory element comprises a variable resistive element 110 sandwiched by a pair of electrodes 108 and 112, where the variable resistive element 110 is formed of CMR materials, perovskite materials, PCMO, LSMO, GBCO or other CMR oxide (column 7, lines 17-23, and column 8, lines 19-22), and the electrodes are formed of metals, metallic oxides, polymers, or mixtures or combinations thereof, Pt, Ag, Au, LaSrCoO.sub.3, YBa.sub.2 Cu.sub.3 O.sub.7-x, RuO.sub.2, IrO.sub.2, SrRuO.sub.3, Al, Ta, TaSiN, MoN doped polyacetylene, polypyrrole, polyaniline, or mixtures or combinations thereof (column 7, lines 10-16).

Specifically, with reference to **claim 1**, the '332 patent discloses a conductive memory device comprising:

a conductive bottom electrode (108);

a multi-resistive state element (110) arranged on top of and in contact with the bottom electrode, the multi-resistive state element having a resistivity; and

a conductive top electrode (112) arranged on top of and in contact with the multi-resistive state element;

wherein the resistivity of the multi-resistive state element may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes (Abstract); and

wherein at least one of the conductive electrodes (formed of a refractory metal nitride or a refractory metal oxide such as TaSiN, MoN, IrO_2, and RuO_2, as detailed above) functions as a barrier layer. Note that although the '332 patent does not explicitly disclose that the conductive electrodes formed of a refractory metal nitride or a refractory metal oxide function as a barrier layer, they function as a barrier layer as is known in the art and as will be explained in details in the paragraphs that follow.

Regarding **claims 8-10**, the '332 patent further discloses that the at least one of the conductive electrodes that functions as a barrier layer includes the ternary nitride TaSiN (tantalum silicon nitride) as claimed. And although not explicitly disclosed, the disclosed ternary nitride TaSiN, just as the claimed ternary nitride TaSiN, reduces either metal diffusion, oxygen diffusion, hydrogen diffusion, or some combination thereof.

Referring to **claims 14 and 18-19**, the '332 patent further discloses that the at least one of the conductive electrodes that functions as a barrier layer includes ternary oxide $SrRuO_3$ and that ternary oxide $SrRuO_3$, being included in the conductive electrode, is a conductive oxide although not explicitly disclosed.

Referring to **claim 21,** the limitation "is oxidized during fabrication" of "the conductive oxide is a conductive metal that is oxidized during fabrication" is taken to be a product-by-process limitation and is considered non-limitation in a product claim (MPEP 2112.01 and MPEP 2113). In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product, the ternary conductive oxide $SrRuO_3$, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a

rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. As for the limitation "remains conductive after oxidation", the conductive oxide of the conductive electrode shall remain conductive for the device to function.

Referring to **claim 22**, as cited above, the metal is Ir or Ru.

Referring to **claim 32**, which recites: "the top electrode, the multi-resistive state element, and the bottom electrode each have similar coefficients of thermal expansion", the top electrode, the multi-resistive state element, and the bottom electrode of the conductive element of the '332 patent each is a metal oxide having an atomic weight similar to those of the others and therefore each has a coefficient of thermal expansion similar to those of the others, whereby the conductive memory element does not experience significant stress from dissimilar coefficients of thermal expansions during normal operation.

Claim Rejections - 35 USC § 102 and 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. **Claims 2, 17, 20, 23-26, 37, and 43** are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over the '332 patent.

Referring to **claim 17**, as mentioned above, the '332 patent discloses ternary conductive oxides such as $SrRuO_3$, metals, metal oxides and mixtures and combinations thereof for

conductive electrodes (108 or 112), and since the '332 patent does not exclude the use of a separate barrier layer (in addition to the conductive electrode layer), it would appear that the ternary oxide of the conductive electrode 108 or 112 could function as a sacrificial barrier (i.e., as a separate barrier layer), and since the disclosed ternary oxide and the claimed ternary oxide is of the same or similar material, the ternary oxide disclosed by the '332 patent would function as a high-temperature oxygen barrier. As for the limitation "at least one of the conductive electrodes remains conductive", the conductive electrodes should remain conductive for the device to function.

Referring to **claims 2 and 25**, since the materials or combinations of the materials of the '332 patent's device are similar to those used by the present invention, as cited above, the multi-resistive state element appears to be fabricated with high temperature processes.

Referring to **claim 20**, the '332 patent discloses RuO_2 , IrO_2, metal, metal oxides and mixtures and combinations thereof, as cited above, and since the reference does not exclude the possibility of the metal and the metal oxide being the same metal, it appears that the metal and the metal oxide could be the same metal.

With respect to the claimed limitations of claims **23-24 and 26**, the conductive oxide of the '332 patent, being formed of the same or similar materials as claimed, could function as claimed.

Referring to **claim 37**, although the '332 patent does not disclose that the at least one of the conductive electrodes that functions as a barrier layer is the bottom electrode and the top electrode is a non-oxidized metal, the reference teaches that, as cited above, suitable electrode materials include, without limitation, metals, metallic oxides, polymers, or mixtures or

combinations thereof. Therefore, the at least one of the conductive electrodes (the metal oxide) that functions as a barrier layer could be the bottom electrode, and the top electrode could be a metal (a non-oxidized metal).

Referring to the limitation "a plurality of x-direction conductive lines in oriented in one direction; a plurality of y-direction conductive lines in a different direction as the x-direction conductive lines, and crossing the x-direction conductive lines; at least one memory array formed by memory cells placed substantially at the intersections of the x-direction conductive lines and y-direction conductive lines" of **claim 41**, as noted above, the '332 patent discloses a memory element array including a plurality of the memory elements formed on a substrate in a column-row or array format. Thus, the memory array shall include X-conducting lines and Y-conducting lines and the cells should be placed substantially at the intersections of the x-direction conductive lines and y-direction conductive lines.

Referring to **claim 43**, each memory cell includes a conductive metal oxide memory element (such as PCMO as cited above) that stores an adjustable resistive value.

Claim Rejections - 35 USC § 103

7. **Claims 35-36** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '053 publication for being obvious.

The '053 publication discloses a conductive memory device as claimed and as detailed above including the insulating barrier 12 including silicon nitride, but fails to disclose that the insulating barrier 12 includes aluminum oxide or tantalum oxide. Nevertheless, the reference teaches in paragraph [0035] that insulating barrier 12 could include any suitable oxides and

nitrides. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form insulating barrier 12 including aluminum oxide or tantalum oxide, oxides suitable for insulating barriers. One would have been motivated to make such a modification because the '053 publication teaches that insulating barrier 12 could include any suitable oxides and nitrides.

8. **Claim 3-7, 11-13, and 15-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '332 patent for being obvious.

Referring to **claims 3 and 4**, the '332 patent discloses a conductive memory device as claimed and as detailed above including the conductive electrodes (108 and 112), at least one of which functions as a barrier layer, but instead of using titanium nitride (TiN) as a material to form the at least one of the conductive electrodes as claimed, the '332 patent discloses using TaSiN. However, TaN or TaSiN functions as a diffusion barrier layer and an adhesive layer (see, for example, U.S. Patent 6,346,475 to Suzuki et al., column 8, lines 15-18) and TiN and TaN (tantalum nitride) are known to function as an adhesive and a barrier layer (see, for example, U.S. Patent 5,668,054 to Sun et al. in the Technical Background Section). Since TaN and TaSiN are art-equivalent materials and TiN and TaN are art equivalent materials, it follows that TaSiN and TiN are art-equivalent materials. Since the materials are art-equivalent, the change of the materials would have been obvious to one of ordinary skill in the art. Note also that all of these metal nitrides are refractory metal nitrides.

With respect to **claims 5-7**, similarly as detailed above being art-equivalent materials, the disclosed binary nitride MoN is functionally equivalent to the claimed titanium nitride or tantalum nitride as claimed (they are all refractory metal nitrides).

Referring to **claims 11-13**, the '332 patent discloses a conductive memory device as claimed and as detailed above including the ternary nitride conductive electrode (108 or 112) formed of TaSiN but the '332 patent's ternary nitride does not include one component that is either ruthenium or iridium and another component that is either tantalum or titanium, or to be specific, the '332 patent discloses TaSiN instead of RuTiN (ruthenium titanium nitride) as claimed. Nevertheless, either of the two ternary nitrides (TaSiN and RuTiN) functions as a conductive barrier layer as is known in the art and as is disclosed by Choi U.S. Patent Application Publication 20030042609 (paragraph [0039]), as an example. Since the materials are art-equivalent, the change of the materials would have been obvious to one of ordinary skill in the art. As for the limitation "the ternary nitride functions as a sacrificial high-temperature oxygen barrier" of **claim 13**, since the '332 patent does not exclude the use of a separate barrier layer (in addition to the conductive electrode layer), it would appear that the ternary nitride of the conductive electrode 108 or 112 could function as a sacrificial barrier (i.e., as a separate barrier layer), and since the disclosed ternary nitride and the claimed ternary nitride is of the same or similar material, the ternary nitride disclosed by the '332 patent would function as a high-temperature oxygen barrier.

Referring to **claims 15-16**, the '332 patent discloses a conductive memory device as claimed and as detailed above including the ternary oxide conductive electrode (108 or 112) formed of $SrRuO_3$ but the '332 patent's ternary oxide does not have one component that is either

ruthenium or iridium and another component that is either tantalum or titanium. To be specific, the '332 patent discloses $SrRuO_3$ instead of RuTa O_x (ruthenium tantalum oxide) as claimed. However, as should be apparent by now, $SrRuO_3$ and RuTa O_x, being refractory metal ternary oxides, are functionally equivalents.

9. **Claims 29-31** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '332 patent in view of the '053 publication.

The '332 patent discloses a conductive memory device as claimed and as detailed above including the multi-resistive state element and the conductive electrode (108 or 112) that comprises platinum (Pt) and a conductive barrier oxide and that functions as a barrier layer (metal, such as Pt, metal oxides, such as RuO_2, and mixtures and combinations thereof), as cited above, but fails to disclose that the layer of metal is in between the conductive oxide and the multi-resistive state element. The '053 publication, also as detailed above, teaches that the layer of metal (top electrode 26) could be formed between the conductive barrier (tungsten nitride) and the multi-resistive state element or that the conductive barrier could be formed between the layer of metal and the multi-resistive state element (as detailed above), thereby teaching that the relative positions of the three layers, i.e., the conductive barrier, the metal layer, and the multi-resistive state element, are art-recognized equivalents. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layers of the '332 patent in the claimed order. One would have been motivated to make such a modification in view of the suggestion in the '053 publication that the various orders of the layers are considered art-recognized equivalents.

Referring to **claim 31**, if the order of the various art-recognized equivalent orders is such that the layer of metal is in between the conductive oxide and the multi-resistive state element, then the layer of metal, which is Pt, should introduce a non-linearity in the IV characteristics of the conductive memory device.

Allowable Subject Matter

10. **Claim 27** (and dependent **claim 28)** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a conductive memory device having all limitations as recited in claims 1, 18, and 27, characterized in that the at least one of the conductive electrodes that functions as a barrier layer includes a conductive oxide and is the bottom electrode, and the bottom electrode functions as a seed layer to the multi-resistive state material.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
August 21, 2004